IN THE SPECIFICATION:

Please amend paragraph **[0046]** as follows:

[0046] In FIG. 3, at least one semiconductor device 12 is provided. As shown, a semiconductor substrate 11 on which a plurality of semiconductor devices 12 (semiconductor devices 12a, 12b being shown) ~~are carried~~ is carried may be provided. By way of example only, semiconductor substrate 11 may comprise a full or partial wafer of semiconductive material (*e.g.*, silicon, gallium arsenide, indium phosphide, etc.), a so-called silicon-on-insulator (SOI) type substrate (*e.g.*, silicon-on-ceramic (SOC), silicon-on-glass (SOG), silicon-on-sapphire (SOS), etc.), or a single-device or multiple-device section of any of the foregoing substrates.

Please amend paragraph **[0050]** as follows:

[0050] Alternatively, as shown in FIG. 4A, discrete lower sections 36a and 36b of contact pads 30 (FIGs. 1 and 2) may be preformed on surface 52 of sacrificial substrate 50, as known in the art. Discrete lower sections 36a and 36b may, as depicted, have chamfered ~~edges 37.~~ edges 38. Such chamfering of ~~edges 37~~ edges 38 of discrete lower sections 36a and 36b may provide a larger surface area than that provided by squared edges, ensuring that subsequently fabricated conductive structures will make adequate electrical contact to discrete lower sections 36a and 36b. Additionally, discrete lower sections 36a and 36b ~~have~~ having chamfered ~~edges 37~~ edges 38 may facilitate the formation of chip-scale packages 10 (FIGs. 1 and 2) from semiconductor substrates 11 (FIG. 3) with relatively narrow streets S. Of course, discrete lowered sections 36a and 36b with squared ~~edges 37~~ edges 38 are also within the scope of the present invention.

Please amend paragraph **[0057]** as follows:

[0057] As shown in FIGs. 9 and 9A, cut lines 58 are formed between adjacent semiconductor devices 12a, 12b. Like cut lines 56 (FIG. 6), cut lines 58 may be formed by use of a wafer saw, laser cutting or machining ~~techinques,~~ techniques, mask and etch processes, or otherwise, as known in the art and suitable for use with the type of material from which dielectric layer 18′ is formed. Again, the use of laser cutting techniques is particularly desirable when the

formation of relatively narrow cut lines 58 of particular depth is desired. Cut lines 58, which are thinner or narrower than cut lines 56, extend through the electrically insulative material of dielectric layer 18', which is located between adjacent semiconductor devices 12a and 12b, leaving a peripheral dielectric coating 60 of the electrically insulative material on outer periphery 15a, 15b of semiconductor devices 12a and 12b. Also, cut lines 58 extend into and substantially through precursor pads 36' exposing at least one edge 38 of the resulting lower section 36 of contact pad 30 (FIGs. 1 and 2). It is currently preferred that, to optimize the robustness of the process described herein, particularly when sacrificial substrate 50 comprises a relatively weak material or when different temperature profiles are used to effect different aspects of the process (*i.e.*, sacrificial substrate 50 is subjected to thermal stresses), cut lines 58 do not extend into sacrificial substrate 50. In the example illustrated in FIG. 9, each precursor pad 36' is severed into two lower sections 36 of contact pads 30, each corresponding to the semiconductor device 12a, 12b beneath which it is located. In the example shown in FIG. 9A, cut lines 58 extend to discrete lower sections 36a and 36b, exposing ~~edges 37~~ edges 38 thereof. Also as a result of the formation of cut lines 58, dielectric layer 18' is severed into a plurality of dielectric layers 18, one for each semiconductor device 12a, 12b.

Please amend paragraph **[0065]** as follows:

[0065] Accordingly, semiconductor device 112 includes a sensing/emission area or region 170 which is exposed to an active surface 113 thereof. Additionally, to protect sensing/emission ~~area~~ region 170, chip-scale package 110 includes an optically transparent lid 172 over at least a portion of sensing/emission ~~area or~~ region 170. Semiconductor device 112 also includes bond pads 116 on active surface 113 thereof, positioned between sensing/emission ~~area~~ region 170 and outer peripheral edge 115 (also referred to as "outer periphery 115").

Please amend paragraph **[0068]** as follows:

[0068] Redistribution layer 120 includes upper sections 132 of contact pads 130. Redistribution layer 120 may also include a plurality of circuits 122 that extend from bond pads 116 to upper ~~portions~~ sections 132 of corresponding contact pads 130.

Please amend paragraph **[0082]** as follows:

[0082] As an alternative to securing a single optically transparent lid 172′ over semiconductor substrate 111, a plurality of individual optically transparent lids 172 may be positioned over sensing/emission ~~area~~ region 170 of each semiconductor device 112 and secured to semiconductor device 112 with an optical grade adhesive 174, as known in the art and as depicted in FIG. 24A.

Please amend paragraph **[0083]** as follows:

[0083] Referring now to FIG. 25, cut lines 158 are formed along the streets between adjacent semiconductor devices 112a and 112b. As depicted, each cut line 158 is aligned with a corresponding cut line 156 and is thinner, or narrower, than its corresponding cut line 156. As such, a peripheral dielectric coating 160 of the material of dielectric layer 118′ remains on outer periphery 115 of each semiconductor device 112a, 112b, etc., so as to electrically insulate the same from a subsequently formed peripheral section 134 of each contact pad 130 (FIGs. 15 and 16). In addition, each cut line 158 exposes a peripheral edge 133 of upper section 132 of each contact pad 130, as well as peripheral ~~edge 137~~ edge 138 of lower section 136 of each contact pad 130.

Please amend paragraph **[0085]** as follows:

[0085] When upper precursor pads 132′ or precursor pads 136′ are present, the technique for forming cut lines 158 should also be suitable for removing the material of such precursor pads 132′, 136′. Of course, when precursor pads 132′ or 136′ are severed during the formation of a cut line 158, they are bisected or otherwise split into upper sections 132a, 132b (collectively, upper sections 132) or lower sections 136a, 136b (collectively, lower sections 136) that are located on active surface 113 or back side 114 of adjacent semiconductor devices 112a, 112b, respectively, with peripheral edges 133, ~~137~~ 138 being formed at each edge of that cut line 158.

Please amend paragraph **[0090]** as follows:

[0090] As depicted, conductive layer 164 overlies semiconductor devices 112a, 112b (being located over optically transparent lids 172 that are disposed thereover), as well as lines peripheral dielectric coatings 160, which form the lateral surfaces of each cut line 158. Additionally, peripheral edges 133 of upper sections 132 of contact pads 130 (FIGs. 15 and 16) and ~~edges 137~~ edges 138 of lower sections 136 of contact pads 130, which are located within cut lines 158, are contacted by portions 166 of conductive layer 164 that are located within cut lines 158.

Please amend paragraph **[0099]** as follows:

[0099] In FIG. 33, a conductive layer 164 is formed over sacrificial layer 163 and on peripheral dielectric coating 160 at each lateral edge of each cut line 158″. As an example only, conductive layer 164 may be formed by the processes that are described herein with reference to FIG. 26. As each bevel cut 176 forms an opening to its corresponding cut line 158″ which is significantly larger than the opening of cut line 158 shown in FIG. 26, bevel cuts 176 may improve the deposition of conductive layer 164 on peripheral dielectric coatings 160 within cut line 158″. Additionally, edges ~~133′of~~ 133′ of upper sections 132 of contact pads 130 (FIGs. 15 and 16) and ~~edges 137~~ edges 138 of lower sections 136 of contact pads 130, which are located within cut lines 158″, are contacted by portions 166 of conductive layer 164 that are located within cut lines 158″.

Please amend paragraph **[00103]** as follows:

[00103] In FIGs. 36 and 39, chip-scale package 10, 110, 110″ is positioned over carrier substrate 210 with a bottom surface 14″ of chip-scale package 10, 110, 110″ facing an upper surface 213 of carrier substrate 210. Intermediate conductive elements 220, 220″, which are respectively shown as being conductive balls (*e.g.*, solder balls) and larger, nonspherical conductive structures, but which may alternatively comprise bumps, columns, pillars, or pins of solder, another metal, conductive or conductor-filled epoxy, or any other suitable conductive material, or which may comprise z-axis conductive elements of a film of anisotropic conductive film, are positioned between bottom surface 14″ of chip-scale package 10, 110, 110″ and upper surface 213 of carrier substrate 210. As shown, intermediate conductive elements 220, 220″ extend between and contact lower sections 36, 136 of contact pads 30, 130 of chip-scale package 10, 110, 110″ and corresponding terminals 230 of carrier substrate 210.